W83176R-400

W83176G-400

Winbond Current Mode
Differential Buffer
for PCI Express and SATA

Date: May/16/2006 Revision: 0.6

W83176R-400/W83176G-400 Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	05/11/04	0.5	n.a.	First publish
2	7	05/16/06	0.6	n.a.	Add lead free part
3					
4					
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CURRENT MODE DIFFERENTIAL BUFFER FOR PCI EXPRESS AND SATA

1. GENERAL DESCRIPTION

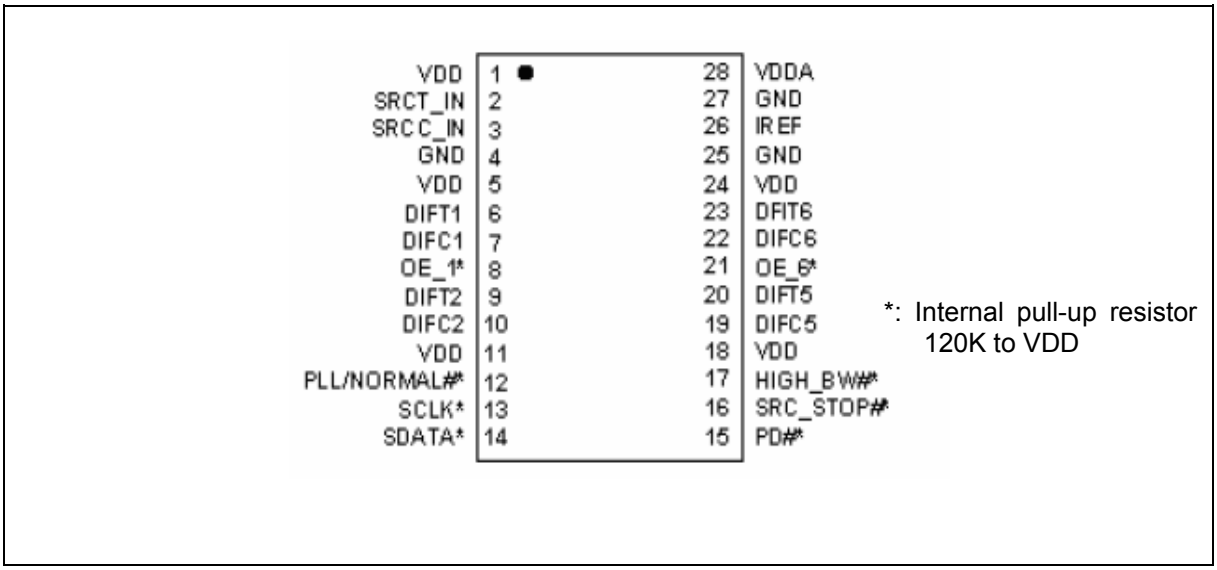
The W83176R-400 supports four current mode differential Clock pair's buffer output companion devices to CK409 or CK410 clock generator.

The W83176R-400 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-400 accepts a reference clock as its input current mode differential pair's clock.

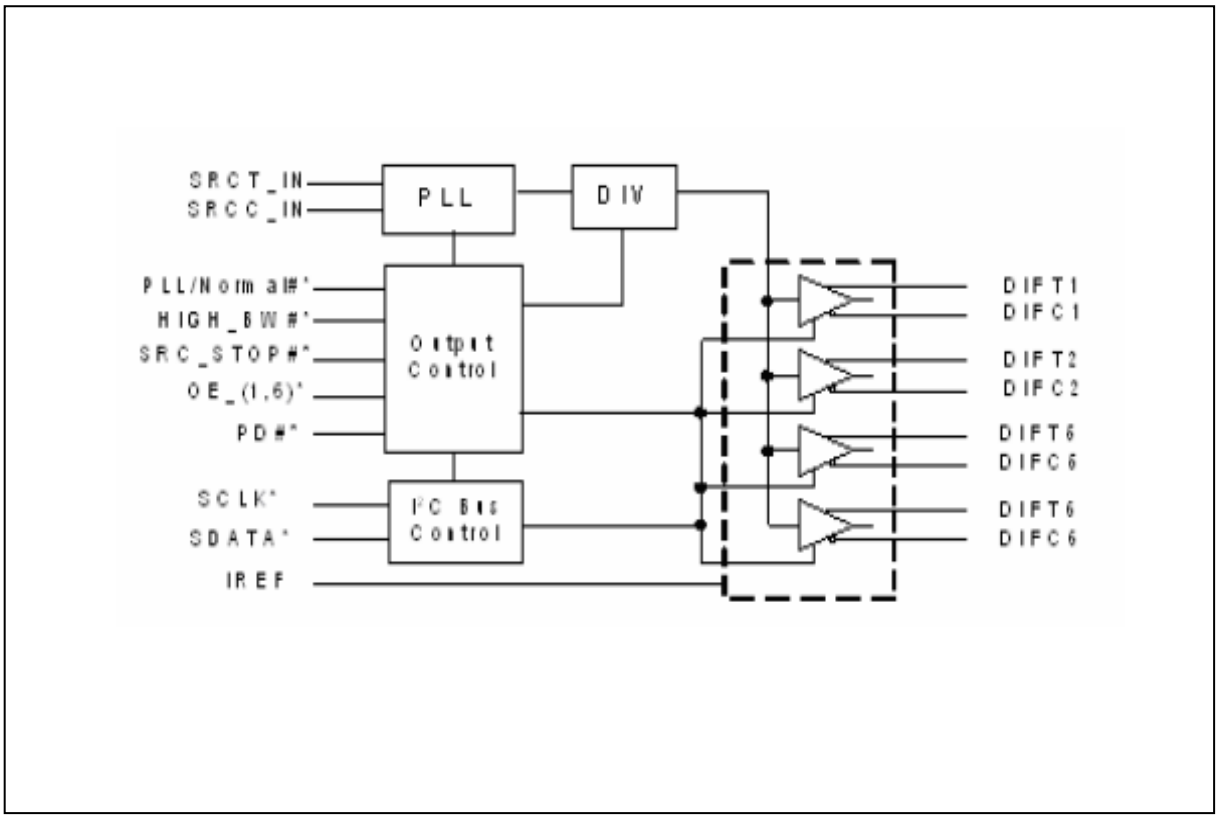
2. PRODUCT FEATURES

- Four current mode differential clock pairs clock outputs
- Support zero delay buffer mode and normal buffer mode
- Supports two hardware output enable/disable pin
- Programmable PLL bandwidth
- Low Skew outputs (< 50ps)
- Low cycle to cycle jitter (<100ps)
- I^2C 2-Wire serial interface and supports Byte or Block Data R/W
- 28-pin SSOP package

3. PIN CONFIGURATION



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
OUT	Output
IN_{tp120k}	Latched input at power up, internal 120kΩ pull up.
*	Internal 120kΩ pull-up
#	Low Active

5.1 Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
2,3	SRCT_IN SRCC_IN	IN	SRC Differential clock input
6,9,20,23,	DIFT (1,2,5,6)	OUT	True Clocks of differential pair outputs
7,10,19,22	DIFC (1,2,5,6)	OUT	Complement Clocks of differential pair outputs
8,21	OE (1,6)*	IN	DIFT/C (1, 6) output control, 0=Tri-state, 1=Enable output, This is internal 120K pull up.
13	SCLK *	IN	Serial clock of I^2C 2-wire control interface Internal pull-up resistor 120K to VDD
14	SDATA *	I/O	Serial data of I^2C 2-wire control interface Internal pull-up resistor 120K to VDD
15	PD#*	IN	Active low to power down the device into low power state is stopped VCO and all output buffers, This is internal 120K pull up.
16	SRC_STOP#*	IN	Active low to stop differential output buffers, This is internal 120K pull up.
17	HIGH_BW#*	IN_{tp120k}	Latched input at power up to selecting PLL Band Width 0=HIGH, 1=LOW, This is internal 120K pull up.
26	IREF	OUT	Deciding the reference current for the Differential clock pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value for 0.7V differential clock output.

5.2 Power Pins

PIN	PIN NAME	DESCRIPTION
4,25,27	GND	Ground
1,5,11,18,24	VDD	Power Supply 3.3V
28	VDDA	Analog power supply, 3.3V

6. I²C CONTROL AND STATUS REGISTERS

6.1 Register 0: Control Register (Default: 07h)

BIT	NAME	PWD	DESCRIPTION
7	PD_DM	0	PD# Drive mode, 0:driven, 1:Hi-Z
6	SRC_ST_DM	0	SRC_STOP Drive mode, 0:driven, 1:Hi-Z
5	SEL_SRCDIV	0	0:control by pin, 1:control by I2C
4	SEL_NORMAL	0	0:control by pin, 1:control by I2C
3	SEL_PLLBW	0	0:control by pin, 1:control by I2C
2	PLL_BW_ ADJ	1	0:High BW, 1:Low BW
1	NORMAL#/PLL	1	0:Normal buffer, 1:PLL mode
0	SRC_DIV#	1	0:Divided by 2 mode, 1:Normal (output=input)

6.2 Register 1: Control Register (Default: FFh)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	DIF6_EN	1	0:Disabled (Hi-Z), 1:Enable
5	DIF5_EN	1	0:Disabled (Hi-Z), 1:Enable
4	Reserved	1	Reserved
3	Reserved	1	Reserved
2	DIF2_EN	1	0:Disabled (Hi-Z), 1:Enable
1	DIF1_EN	1	0:Disabled (Hi-Z), 1:Enable
0	Reserved	1	Reserved

6.3 Register 2: Control Register (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	DIF6STOP_EN	0	0:Free-run, 1:Stoppable
5	DIF5STOP_EN	0	0:Free-run, 1:Stoppable
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	DIF2STOP_EN	0	0:Free-run, 1:Stoppable
1	DIF1STOP_EN	0	0:Free-run, 1:Stoppable
0	Reserved	0	Reserved

6.4 Register 3: Reserved Register (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	Reserved	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	Reserved	0	Reserved

6.5 Register 4: Winbond Chip ID – Project Code Register (Default: 11h)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83176R-400 (SA5911).
6	CHPI_ID [6]	0	Winbond Chip ID.
5	CHPI_ID [5]	0	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	0	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

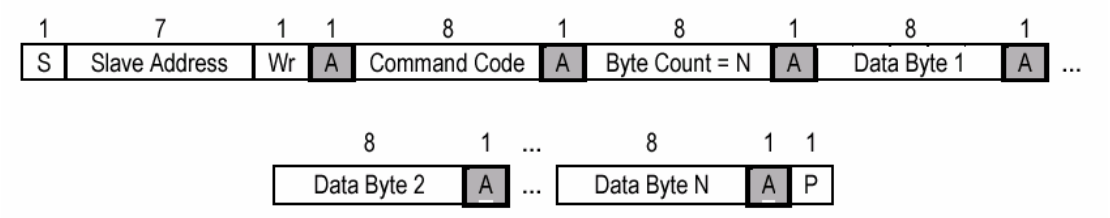
6.6 Register 5: Test Register (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	TEST1	0	Reserved
6	TEST0	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	Reserved	0	Reserved

7. ACCESS INTERFACE

The W83176R-400 provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83176R-400 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C write address is defined at 0xDC. The I^{2}C read address is defined at 0xDD.

7.1 Block Write protocol

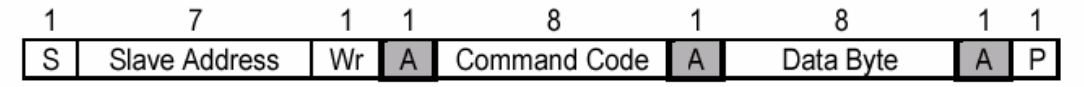


7.2 Block Read protocol

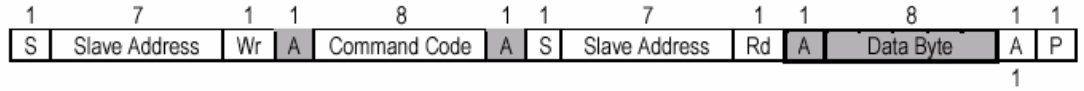


In block mode, the command code must filled '00h'

7.3 Byte Write protocol



7.4 Byte Read protocol

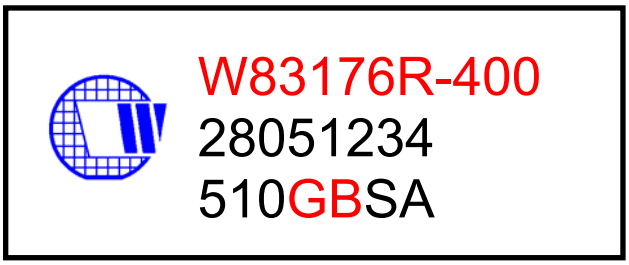


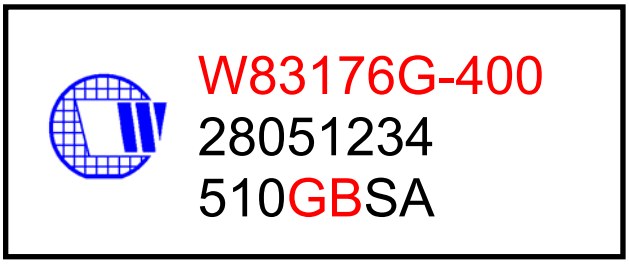
In Byte Mode, the index No= (Register No) + 1

8. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83176R_400	28 PIN SSOP	Commercial, 0°C to +70°C
W83176G-400	28 PIN SSOP (Lead free package)	Commercial, 0°C to +70°C

9. HOW TO READ THE TOP MARKING



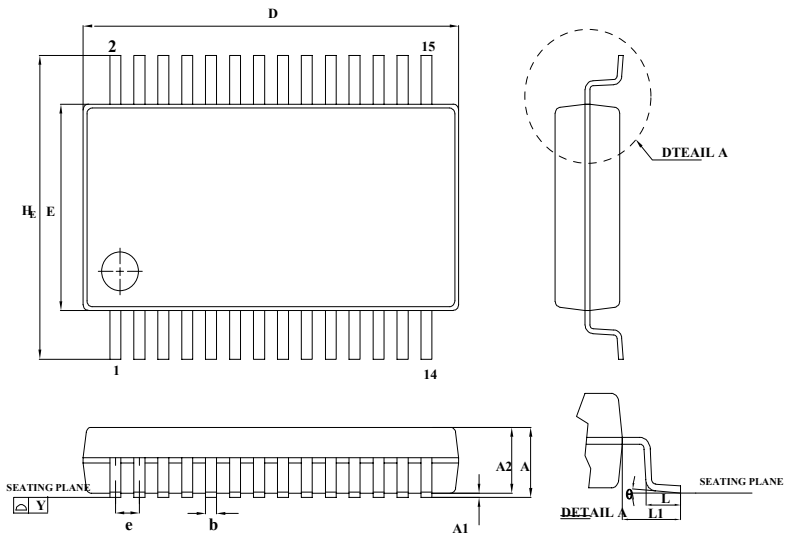


1st line: Winbond logo and the type number:
Normal part: W83176R-400, Lead free part: W83176G-400
2nd line: Tracking code 2 8051234
2: wafers manufactured in Winbond FAB 2
8051234: wafer production series lot number
3rd line: Tracking code 418 G B SA
510: packages made in '2005, week 10
G: assembly house ID; O means OSE, G means GR
B: IC revision
SA: Winbond Internal use

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10. PACKAGE DRAWING AND DIMENSIONS

28pin 209mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	9.90	10.20	10.50	0.389	0.401	0.413
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

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